

IN THE CLAIMS

Please add the following claims:

15. A receiver circuit arranged in a receiving unit  
of multiplex radio equipment, said receiving unit including  
an identifying circuit for identifying a signal at a  
predetermined identification level, said signal being  
obtained by demodulating a multilevel orthogonal modulated  
signal, an equalizing circuit for subjecting said  
demodulated signal to an equalizing process, and a clock  
regenerating circuit regenerating a signal identification  
clock for said identifying circuit and then supplying said  
signal identification clock to said identifying circuit;  
comprising:

a clock regenerating unit for regenerating said signal  
identification clock based on a signal before said  
multilevel orthogonal modulated signal is detected;

a phase adjusting unit for adjusting the phase of a  
clock from said clock regenerating unit and then supplying  
the phase-adjusted clock to said identifying circuit; and

a clock phase detecting unit for detecting a phase  
component of said signal identification clock based on

*and the output signal*  
*the* input/output signals of said equalizing circuit and then  
supplying the result as a phase adjustment control signal  
to said phase adjusting unit.

*A*  
16. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 15,  
further comprising an averaging unit arranged between said  
clock phase detecting unit and said phase adjusting unit,  
for averaging the output from said clock phase detecting  
unit.

*not shown*

17. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 15,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulation signal; and wherein said  
clock regenerating unit, said phase adjusting unit, and  
said clock phase detecting unit are used in common to said  
plural identifying units.

*112 25T  
not shown -  
Fig 28-42*

18. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 15,  
wherein said identifying circuit comprises plural

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identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulation signal; and further  
comprising an averaging unit arranged between said clock  
phase detecting unit and said phase adjusting unit, for  
averaging the output from said clock phase detecting unit;  
and wherein said clock regenerating unit, said phase  
adjusting unit, said averaging unit, and said clock phase  
detecting unit are used in common to said plural  
identifying units.

*112 25A  
not shown*

*112 25A*

19. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 15,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulation signal; and wherein said  
clock regenerating unit is shared among said plural  
identifying units; and wherein plural phase adjusting units  
and plural clock phase detecting units are arranged  
corresponding to said plural identifying units.

*N.A.*

20. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 15,

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wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit; said clock regenerating unit is used in common to said plural identifying units; and a plurality of said phase adjusting units, said averaging units and said clock phase detecting units are arranged corresponding to said plural identifying units.

*21*

21. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 15, further comprising a test signal generating unit for generating a test signal; and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said test signal generating unit, said output of said selecting unit being supplied as an input to said phase adjusting unit.

*112 45A*

22. A receiver circuit arranged in a receiving unit of multiplex radio equipment, said receiving unit including

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal, an equalizing circuit for subjecting said signal obtained by demodulating a multilevel orthogonal modulated signal <sup>the</sup> and an equalizing circuit to an equalizing process, and a clock regenerating circuit regenerating a signal identification clock for said identifying circuit and then supplying said signal identification clock to said identifying circuit; comprising:

a clock phase detecting unit for detecting a phase component of said signal identification clock based on <sup>the signal and the signal</sup> signals input to or output from said equalizing circuit; a loop filter unit for integrating the output from said clock phase detecting unit; and an oscillating unit for producing <sup>said</sup> a signal identification clock for said identifying circuit to said identifying circuit, in response to as a control input <sup>the output of</sup> the output from said loop filter unit.

23. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 22, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

demodulated signals obtained by demodulating said  
multilevel orthogonal modulation signal; and wherein said  
clock phase detecting unit, said loop filter unit, and said  
oscillating unit are used in common to said plural  
identifying units.

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24. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 22,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein plural  
clock phase detecting units are arranged to said  
identifying units; and wherein said loop filter unit and  
said oscillating unit are used in common to said  
identifying units; and further comprising a composing unit  
for composing the outputs of said clock phase detecting  
units to input the resultant output of said composing unit  
to said loop filter unit.

112 154

25. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 22,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural

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demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and further  
comprising plural clock phase detecting units and plural  
loop filter units being arranged corresponding to said  
plural identifying units; said oscillating unit being used  
in common to said plural identifying units; a part of said  
plural identifying units being connected to said  
oscillating unit via said phase adjusting unit, said output  
of said loop filter unit being supplied as a control input  
to said oscillating unit or said phase adjusting unit.

*112 257*

*112 257*

26. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 22,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein said  
loop filter unit and said oscillating unit are used in  
common to said plural identifying units; and further  
comprising a second clock phase detecting unit for  
detecting the phase component of said signal identification  
clock in a method <sup>?</sup> different from that of said clock phase  
detecting unit and a composing unit for composing the  
output from said clock phase detecting unit with the output



from said second clock phase detecting unit, the output of  
said composing unit being supplied as an input to said loop  
filter unit.

27. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 22,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein said  
loop filter unit and said oscillating unit are used in  
common to said plural identifying units; and further  
comprising a second clock phase detecting unit for  
detecting the phase component of said signal identification  
clock in a method different from that of said clock phase  
detecting unit and a selecting unit for selectively  
producing the output from said clock phase detecting unit  
and the output from said second clock phase detecting unit,  
the output of said selecting unit being supplied as an  
input to said loop filter unit.

28. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 22,  
further comprising a test signal generating unit for



generating a test signal; and a selecting unit for  
selectively producing the output from said clock phase  
detecting unit and the output from said test signal  
generating unit, said output of said selecting unit being  
supplied as an input to said loop filter unit.

29. A receiver circuit arranged in a receiving unit  
of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a  
predetermined identification level, said signal being  
obtained by demodulating a multilevel orthogonal modulated  
signal;

a clock regenerating circuit for regenerating a signal  
identification clock for said identifying circuit to supply  
said clock to said identifying circuit; and

a clock phase detecting unit for detecting a phase  
component of said signal identification clock based on  
clock phase difference information supplied to said  
identifying circuit and signal error differential  
information obtained by said identifying circuit and then  
supplying said resultant phase component to said clock  
regenerating circuit.

30. The receiver circuit arranged in a receiving unit

of multiplex radio equipment, according to claim 29,  
wherein said clock phase detecting unit comprises:

a clock phase difference detecting unit for detecting  
said clock phase difference information supplied to said  
identifying circuit;

a signal error differential detecting unit for  
detecting signal error differential information obtained by  
said identifying circuit; and

a clock phase calculating unit for calculating the  
phase component of said signal identification clock based  
on the output from said clock phase difference detecting  
unit and the output from said signal error differential  
detecting unit.

31. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 29,  
wherein said clock phase <sup>N.A</sup>calculating unit comprises a  
dividing unit that subjects the output of said <sup>N.A</sup>error  
detecting unit and the output of said <sup>N.A</sup>signal inclination  
detecting unit to a dividing calculation process.

32. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 29,  
wherein said clock phase <sup>N.A</sup>calculating unit is formed as an

exclusive OR calculating unit that subjects the output of  
said error detecting unit <sup>N. 17</sup> and the output of said signal  
inclination detecting unit <sup>N. 17</sup> to an exclusive OR calculation  
process.

33. A receiver circuit arranged in a receiving unit  
of multiplex radio equipment, said receiving unit having an  
identifying circuit that identifies a signal obtained by  
demodulating a multilevel orthogonal modulated signal at a  
predetermined identification level, and a clock  
regenerating circuit regenerating a signal identification  
clock for said identifying circuit to supply said clock to  
said identifying circuit, comprising:

a clock regenerating unit for regenerating said  
signal identification clock based on a signal before said  
multilevel orthogonal modulation signal is detected;

a phase adjusting unit for adjusting the phase of a  
clock sent from said clock regenerating unit and supplying  
the resultant clock <sup>N. 17</sup> to said identifying circuit; and

a clock phase detecting unit for detecting a phase  
component of said signal identification clock based on  
clock phase difference information supplied to said  
identifying circuit and signal error differential  
information obtained by said identifying circuit and then

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supplying said resultant phase component to said clock regenerating circuit.

*34.* The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, further comprising an averaging unit arranged between said clock phase detecting unit and said phase adjusting unit, for averaging the output from said clock phase detecting unit.

*35.* The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said clock regenerating unit, said phase adjusting unit, and said clock phase detecting unit are used in common to said plural identifying units.

*36.* The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 33, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural

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demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and further  
comprising an averaging unit arranged between said clock  
phase detecting unit and said phase adjusting unit, for  
averaging the output from said clock phase detecting unit;  
and wherein said clock regenerating unit, said phase  
adjusting unit, said averaging unit, and said clock phase  
detecting unit are used in common to said plural  
identifying units.

*37*

37. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 33,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein said  
clock regenerating unit is used in common to said plural  
identifying units; and wherein plural phase adjusting units  
and plural clock phase detecting units are arranged  
corresponding to said plural identifying units.

38. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 33,  
wherein said identifying circuit comprises plural

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*Cont*  
*SECRET*

identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and further  
comprising an averaging unit arranged between said clock  
phase detecting unit and said phase adjusting unit, for  
averaging the output from said clock phase detecting unit;  
and wherein said clock regenerating unit is used in common  
to said plural identifying units, and a plurality of said  
phase adjusting units, said averaging units and said clock  
phase detecting units are arranged corresponding to said  
plural identifying units.

*SECRET*

*39*

39. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 33,  
further comprising a test signal generating unit for  
generating a test signal; and a selecting unit for  
selectively producing the output from said clock phase  
detecting unit and the output from said test signal  
generating unit, said output of said selecting unit being  
supplied as an input to said phase adjusting unit.

40. A receiver circuit arranged in a receiving unit  
of multiplex radio equipment, said receiving unit including  
an identifying circuit for identifying a signal at a

predetermined identification level, said signal being  
obtained by demodulating a multilevel orthogonal modulated  
signal, and a clock regenerating circuit regenerating a  
signal identification clock for said identifying circuit  
and then supplying said signal identification clock to said  
identifying circuit; comprising:

a clock phase detecting unit for detecting a phase  
component of said signal identification clock based on  
clock phase difference information supplied to said  
identifying circuit and signal error differential  
information obtained by said identifying circuit and  
supplying said phase component to said clock regenerating  
circuit;

a loop filter unit for integrating the output from  
said clock phase detecting unit; and

an oscillating unit for producing a signal  
identification clock for said identifying circuit to said  
identifying circuit, in response to the output as a control  
input from said loop filter unit.

41. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 40,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural



demodulated signals obtained by demodulating said  
multilevel orthogonal modulation signal; and wherein said  
clock phase detecting unit, said loop filter unit, and said  
oscillating unit are used in common to said plural  
identifying units.

42. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 40,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein said  
loop filter unit and said oscillating unit are used in  
common to said identifying units, and plural clock phase  
detecting units are arranged corresponding to said  
identifying units; and further comprising a composing unit  
that composes outputs of said plural clock phase detecting  
units and then supplies the resultant output as an input to  
said loop filter unit.

43. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 40,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural

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demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and further  
comprising plural clock phase detecting units and plural  
loop filter units being arranged corresponding to said  
plural identifying units; said oscillating unit being used  
in common to said plural identifying units; a part of said  
plural identifying units being connected to said  
oscillating unit via said phase adjusting unit<sup>~.1A</sup>, said output  
of said loop filter unit being supplied as a control input  
to said oscillating unit or said phase adjusting unit.

*FIGURE 4*

44. The receiver circuit arranged in a receiving unit  
of multiplex radio equipment, according to claim 40,  
wherein said identifying circuit comprises plural  
identifying units corresponding to the number of plural  
demodulated signals obtained by demodulating said  
multilevel orthogonal modulated signal; and wherein said  
loop filter unit and said oscillating unit are used in  
common to said plural identifying units; and further  
comprising a second clock phase detecting unit for  
detecting the phase component of said signal identification  
clock in a method<sup>?</sup> different from that of said clock phase  
detecting unit and a composing unit for composing the  
output from said clock phase detecting unit with the output

from said second clock phase detecting unit, the output of said composing unit being supplied as an input to said loop filter unit.

45. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said loop filter unit and said oscillating unit are used in common to said plural identifying units; and further comprising a second clock phase detecting unit for detecting the phase component of said signal identification clock in a method<sup>?</sup> different from that of said clock phase detecting unit and a selecting unit for selectively producing the output from said clock phase detecting unit and the output from said second clock phase detecting unit, the output of said selecting unit being supplied as an input to said loop filter unit.

46. The receiver circuit arranged in a receiving unit of multiplex radio equipment, according to claim 40, further comprising a test signal generating unit for

generating a test signal; and a selecting unit for  
selectively producing the output from said clock phase  
detecting unit and the output from said test signal  
generating unit, said output of said selecting unit being  
supplied as an input to said loop filter unit.

→ reads on Figs. 4-6 only (not Figs. 1-3) ?

47. A receiver circuit arranged in a receiving unit  
of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated  
signal at a predetermined identification level, said  
demodulated signal being obtained by demodulating a  
multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal  
identification clock for said identifying circuit to supply  
said signal identification clock to said identifying  
circuit; and

a clock phase detecting section for detecting a phase  
component of said signal identification clock, based on  
clock-phase-detecting composite input information including  
any one of (i) a combination of demodulated signal which is  
obtained by demodulating the multilevel orthogonal  
modulated signal and an equalized demodulated signal and  
(ii) a combination of clock phase <sup>difference</sup> information to be  
supplied to said identifying circuit and signal error